UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/899,573	07/05/2001	Pietro Erratico	99CA39653292	1615

27975 7590 02/27/2004

ALLEN, DYER, DOPPELT, MILBRATH & GILCHRIST P.A.
1401 CITRUS CENTER 255 SOUTH ORANGE AVENUE
P.O. BOX 3791
ORLANDO, FL 32802-3791

EXAMINER	
MONDT, JOHANNES P	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 02/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/899,573	ERRATICO, PIETRO
	Examiner	**Art Unit**
	Johannes P Mondt	2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 December 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12-31* is/are pending in the application.

4a) Of the above claim(s) *27-31* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Amendment filed 12/05/03 forms the basis of this Office Action. In said Amendment Applicant substantially amended claims 12, 17 and 22 (i.e., all independent claims). Claims 1-11 have previously been cancelled while claims 27-31 have previously been withdrawn. Therefore, claims 12-26 are currently being examined. Comments on Remarks in said Amendment are included below under "Response to Arguments".

Response to Arguments

1. Applicant's arguments filed 12/05/03 have been fully considered but they are not persuasive:

(a) With regard to the stated arguments in favor of patentability of the claims due to the newly added limitations underscored on page 10 of Remarks:

(1) Hunter et al as cited do not solely teach an isolating trench "to prevent latch-up in CMOS devices", as appears to be alleged by Applicant (page 10 of Remarks), but clearly refers to both bipolar processes in conjunction with CMOS devices, while the objective of Applicant as stated in the Specification is the prevention of the occurrence of latch-up caused by a parasitic lateral NPN transistor on the CMOS side of the device (see page 7, line 25 – page 8, line 18: region 105 is both the drain of the double diffused MOS (DMOS) transistor and the emitter of said parasitic lateral NPN transistor). For the connection between

parasitic lateral transistor and latch-up see page 3 of the Specification. Therefore, the newly added limitation appears to only further limit the invention by Hunter et al to an obvious application of the isolation trench, as is borne out after further search, as witnessed by the art rejections included below.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. ***Claim 12-13 and 15-16*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hunter et al (4,631,803) in view of Yamaguchi et al (IEEE Journal of Solid-State Circuits, Vol. SC-20 (1), February 1985) and Pfirsch (5,736,445).

Hunter et al teach a substrate 16 having first conductivity type (p-type) and an epitaxial layer 14 on said substrate and having the first conductivity type (p-type) and a conductivity less than that of the substrate (substrate is p+, epi layer is p-) (cf. col. 2, lines 43-45); a first region 12 (cf. col. 2, lines 40-43) in said epi layer of second conductivity type (n-type) opposite to said first conductivity type, said first region extending from a surface of said epi layer opposite said substrate into said epi layer to form a first junction therewith; and an isolation element 36 (cf. Figure 2 and col. 3, lines 21-63) positioned on one side of said first region and extending from the surface of said

epi layer at least as far as the top surface of said substrate (cf. Figure 2), thus inherently reducing an injection of current through said epi layer from said first region to any existing region on the side opposite the trench from said first region in the event a second region of second conductivity with a junction with the epi layer were to exist on said opposite side when the first and second junctions are oppositely biased; said isolation element 36 comprising a dielectric material 38 (cf. col. 3, lines 37-44) adjacent said epi layer and polycrystalline silicon 42 (cf. col. 3, lines 55-62) spaced apart from said epi layer by said dielectric material, said isolating element also terminating above a bottom surface of said substrate (cf. col. 6, line 2).

Hunter et al do not necessarily teach the second region as claimed. However, the purpose of the isolation trench by Hunter et al has clearly been stated to include trench isolation for suppressing latch-up in CMOS devices (cf. col. 1, lines 12-28); therefore, an obvious application of the isolation trench by Hunter et al is to the CMOS device structure of Figure 1 in Yamaguchi et al in which the central trench separates NMOS and PMOS devices, the NMOS device being on the side of the said first region, while the second region is the N+ region biased, in fact: connected, to Vss, while said first region is biased by the gate electrode of the PMOS device. Hence it is seen that the not specifically claimed limitations by Hunter et al are present in an obvious application of the kind for which Hunter et al intended their trench isolation invention.

Motivation to include said teaching by Yamaguchi et al is provided by the intended application by Hunter et al to deep trench isolation of CMOS devices (inter alia) as stated in their “Background”, for the purpose of latch-up suppression (cf. col. 1,

line 24). *Combination* of said teaching with said invention is straightforward because at most the trench already shown by Yamaguchi et al would have to dug a little more deeply into the P+ substrate. *Success* of the implementation of said combination can therefore be reasonably expected.

Furthermore, the pn junctions formed by said first and second regions are normally reversed-biased in that a reverse bias pertains to a normal operational mode of the device; in addition, in this respect, it is pointed out that the bias pertains to a method of using the circuit, not to a limitation carrying patentable weight for the circuit as a device.

Neither Hunter et al nor Yamaguchi et al necessarily teach the additional device limitation that the first region and second region to be power and signal processing sections, respectively, although they are integrated in said epitaxial layer; nor do either Hunter et al not Yamaguchi et al necessarily teach at least one of the said power and signal processing sections to include at least one of a bipolar transistor and a DMOS transistor (i.e., to be either a bipolar transistor or a DMOS transistor). *However, it would have been obvious to include* said additional device limitation in view of Pfirsch, who, in a patent on the production of at least two transistors in one semiconductor body (cf. title and abstract), teach (cf. Figure 2) a DMOS power transistor 40 (cf. Figure legend of Figure 2 and column 6, lines 20-40) and a p-channel MOS transistor 41 for signal processing (cf. Figure 2 and its legend and column 6, lines 20-40) in one and the same semiconductor body. *Motivation*, to include said additional limitation taught by Pfirsch in the device by Hunter et al and Yamaguchi et al, derives from the obviousness of

applying the trench isolation by Hunter et al to the particular MOS transistor that functions as a signal processor side by side on the same chip with a power transistor. In other words: the device by Pfirsch qualifies as an obvious application of the invention by Hunter et al.

Finally, with regard to the added limitation that said reduction of the injection of current through said epitaxial layer from the first region to the second region should take place when the first "junction is biased to cause the injection of current", is a trivial one: without any bias to cause a tendency to injection current the isolating element would not have any function.

On claim 13: in the device of claim 12 as essentially taught by Hunter et al and Yamaguchi et al the isolating element at least partially surrounds said first region (cf. Figure 1 in Yamaguchi et al) which obviously increases improvement of the latch-up protection.

On claim 15: in the device by Hunter et al and Yamaguchi et al the first conductivity type is p-type (see discussion of claim 1).

On claim 16: Although neither Hunter et al nor Yamaguchi necessarily teach the further limitation as defined by claim 16, application of the device by Hunter et al, Yamaguchi et al, i.e., a CMOS device with latchup protection, to power transistors is an obvious application of the invention, as is evident from Pfirsch, who teaches a DMOS power transistor, while it is understood in the art that latchup is a ubiquitous concern for signal processing MOS devices in the presence of high electric potentials. Claim 16 thus merely recites an obvious application of the invention.

3. ***Claim 14*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Hunter et al, Yamaguchi et al and Pfirsch as applied to claim 12 above, and further in view of Nakagawa (6,239465 B1).

As detailed above, Claim 12 is unpatentable over Hunter et al, Yamaguchi et al, and Pfirsch, who do not necessarily teach the further limitation as defined by claim 14. However, Nakagawa teaches isolation trenches for prevention of electrical interference between different portions of the device and with a length substantially equal to the width of the chip (cf. Figures 5 and 8).

Motivation to include the teaching by Nakagawa in the invention of Hunter et al, Yamaguchi et al and Pfirsch is the purpose for which the trench is made, namely: to prevent a current path between the different portion of the device: that is what (electrical) isolation element means. Combination of the inventions is easily accomplished as no other limitation pertains to the direction along the width of the chip while any part of the chip in Hunter et al, Yamaguchi et al and Pfirsch not provided with the trench isolation is clearly not substantial to the invention, said trench isolation being shown on each and every embodiment. For the above reasons it would have been obvious to improve the invention by Hunter et al, Yamaguchi et al and Pfirsch in accordance with the abovementioned teaching by Nakagawa so as to accentuate the role and function of the isolation element as essentially taught by Hunter et al, Yamaguchi et al and Pfirsch.

4. ***Claim 17-21*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Hunter et al (4,631,803) in view of Yamaguchi et al (IEEE Journal of Solid-State Circuits, Vol. SC-20 (1), February 1985) and Pfirsch (5,736,445).

Hunter et al teach a substrate 16 having first conductivity type (p-type) and an epitaxial layer 14 on said substrate and having the first conductivity type (p-type) and a conductivity less than that of the substrate (substrate is p+, epi layer is p-) (cf. col. 2, lines 43-45); a first region 12 (cf. col. 2, lines 40-43) in said epi layer of second conductivity type (n-type) opposite to said first conductivity type, said first region extending from a surface of said epi layer opposite said substrate into said epi layer to form a first junction therewith; and an isolation element 36 (cf. Figure 2 and col. 3, lines 21-63) positioned on one side of said first region and extending from the surface of said epi layer at least as far as the top surface of said substrate (cf. Figure 2), thus inherently reducing an injection of current through said epi layer from said first region to any existing region on the side opposite the trench from said first region in the event a second region of second conductivity with a junction with the epi layer were to exist on said opposite side when the first and second junctions are oppositely biased; said isolation element 36 at least partially surrounding said first region 12 (cf. Figure 2), said isolating element also terminating above a bottom surface of said substrate (cf. col. 6, line 2).

Hunter et al do not necessarily teach the second region as claimed. However, the purpose of the isolation trench by Hunter et al has clearly been stated to include trench isolation for suppressing latch-up in CMOS devices (cf. col. 1, lines 12-28); therefore, an

obvious application of the isolation trench by Hunter et al is to the CMOS device structure of Figure 1 in Yamaguchi et al in which the central trench separates NMOS and PMOS devices, the NMOS device being on the side of the said first region, while the second region is the N+ region biased, in fact: connected, to Vss, while said first region is biased by the gate electrode of the PMOS device. Hence it is seen that the not specifically claimed limitations by Hunter et al are present in an obvious application of the kind for which Hunter et al intended their trench isolation invention.

Motivation to include said teaching by Yamaguchi et al is provided by the intended application by Hunter et al to deep trench isolation of CMOS devices (inter alia) as stated in their "Background", for the purpose of latch-up suppression (cf. col. 1, line 24). *Combination* of said teaching with said invention is straightforward because at most the trench already shown by Yamaguchi et al would have to dug a little more deeply into the P+ substrate. *Success* of the implementation of said combination can therefore be reasonably expected.

Furthermore, the pn junctions formed by said first and second regions are normally reversed-biased in that a reverse bias pertains to a normal operational mode of the device; in addition, in this respect, it is pointed out that the bias pertains to a method of using the circuit, not to a limitation carrying patentable weight for the circuit as a device.

Neither Hunter et al nor Yamaguchi et al necessarily teach the additional device limitation that the first region and second region to be power and signal processing sections, respectively, although they are integrated in said epitaxial layer; nor do either

Hunter et al not Yamaguchi et al necessarily teach at least one of the said power and signal processing sections to include at least one of a bipolar transistor and a DMOS transistor (i.e., to be either a bipolar transistor or a DMOS transistor). *However, it would have been obvious to include* said additional device limitation in view of Pfirsch, who, in a patent on the production of at least two transistors in one semiconductor body (cf. title and abstract), teach (cf. Figure 2) a DMOS power transistor 40 (cf. Figure legend of Figure 2 and column 6, lines 20-40) and a p-channel MOS transistor 41 for signal processing (cf. Figure 2 and its legend and column 6, lines 20-40) in one and the same semiconductor body. *Motivation*, to include said additional limitations taught by Pfirsch in the device by Hunter et al and Yamaguchi et al, derives from the obviousness of applying the trench isolation by Hunter et al to the particular MOS transistor that functions as a signal processor side by side on the same chip with a power transistor. In other words: the device by Pfirsch qualifies as an obvious application of the invention by Hunter et al.

Finally, with regard to the added limitation that said reduction of the injection of current through said epitaxial layer from the first region to the second region should take place when the first "junction is biased to cause the injection of current", is a trivial one: without any bias to cause a tendency to injection current the isolating element would not have any function.

On claim 18: said isolating element 36 comprises a dielectric material (oxide layer 38) (cf. col. 3, lines 40-45).

On claim 19: said isolating element 36 further comprises polycrystalline silicon (cf. col. 3, lines 55-62).

On claim 20: the device of claim 18 as taught by Hunter et al and Yamaguchi et al has p-type for the first conductivity type (see discussion of claims 12 and 17).

On claim 21: Although neither Hunter et al nor Yamaguchi necessarily teach the further limitation as defined by claim 21, application of the device by Hunter et al and Yamaguchi et al, i.e., a MOS device with latchup protection, to power transistors is an obvious application of the invention, as is evident from Pfirsch, who teaches DMOS power transistors, while it is understood in the art that latch-up is a ubiquitous concern for MOS signal processing devices. Claim 21 thus merely recites an obvious application of the invention.

5. ***Claims 22-26*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hunter et al (4,631,803) in view of Yamaguchi et al (IEEE J. Solid-State Circuits, Vol. sc-20 (1), February 1985) and Nakagawa (6,239465 B1).

Hunter et al teach a substrate 16 having first conductivity type (p-type) and an epitaxial layer 14 on said substrate and having the first conductivity type (p-type) and a conductivity less than that of the substrate (substrate is p+, epi layer is p-) (cf. col. 2, lines 43-45); a first region 12 (cf. col. 2, lines 40-43) in said epi layer of second conductivity type (n-type) opposite to said first conductivity type, said first region extending from a surface of said epi layer opposite said substrate into said epi layer to form a first junction therewith; and an isolation element 36 (cf. Figure 2 and col. 3, lines

21-63) positioned on one side of said first region and extending from the surface of said epi layer at least as far as the top surface of said substrate (cf. Figure 2), thus inherently reducing an injection of current through said epi layer from said first region to any existing region on the side opposite the trench from said first region in the event a second region of second conductivity with a junction with the epi layer were to exist on said opposite side when the first and second junctions are oppositely biased; said isolation element 36 also terminating above a bottom surface of said substrate (cf. col. 6, line 2).

Hunter et al nor Yamaguchi et al necessarily teach the further limitation that said isolating element should have "a length substantially equal to a width of the semiconductor chip and dividing the semiconductor chip into two portions each respectively including said first and second regions". However, Nakagawa teaches isolation trenches for prevention of electrical interference between different superficial portions of the device and with a length substantially equal to the width of the chip (cf. Figures 5 and 8) and such that each of said portions include said first and second regions (numeral 28 in Nakagawa; see also Figure 3 in Nakagawa).

Motivation to include the teaching by Nakagawa in the invention of Hunter et al and Yamaguchi et al is the purpose for which the trench is made, namely: to prevent a current path between the different portion of the device: that is what (electrical) isolation element means. Combination of the inventions is easily accomplished as no other limitation pertains to the direction along the width of the chip while any part of the chip in the device by Hunter et al and Yamaguchi et al not provided with the trench isolation is

clearly not substantial to the invention, said trench isolation being shown on each and every embodiment. For the above reasons it would have been obvious to improve the invention by Hunter et al and Yamaguchi et al in accordance with the abovementioned teaching by Nakagawa so as to accentuate the role and function of the isolation element as taught by Hunter et al and Yamaguchi et al.

Furthermore, the pn junctions formed by said first and second regions are normally reversed-biased in that a reverse bias pertains to a normal operational mode of the device; in addition, in this respect, it is pointed out that the bias pertains to a method of using the circuit, not to a limitation carrying patentable weight for the circuit as a device.

Neither Hunter et al nor Yamaguchi et al nor Nakagawa necessarily teach the additional device limitation that the first region and second region to be power and signal processing sections, respectively, although they are integrated in said epitaxial layer; nor do either Hunter et al not Yamaguchi et al necessarily teach at least one of the said power and signal processing sections to include at least one of a bipolar transistor and a DMOS transistor (i.e., to be either a bipolar transistor or a DMOS transistor). *However, it would have been obvious to include* said additional device limitation in view of Pfirsch, who, in a patent on the production of at least two transistors in one semiconductor body (cf. title and abstract), teach (cf. Figure 2) a DMOS power transistor 40 (cf. Figure legend of Figure 2 and column 6, lines 20-40) and a p-channel MOS transistor 41 for signal processing (cf. Figure 2 and its legend and column 6, lines 20-40) in one and the same semiconductor body. *Motivation*, to include said additional

limitation taught by Pfirsch in the device by Hunter et al and Yamaguchi et al, derives from the obviousness of applying the trench isolation by Hunter et al to the particular MOS transistor that functions as a signal processor side by side on the same chip with a power transistor. In other words: the device by Pfirsch qualifies as an obvious application of the invention by Hunter et al.

On claims 23-25: said isolating element by Hunter et al, Yamaguchi, Nakagawa and Pfirsch comprises a dielectric material 38 (cf. col. 3, lines 37-45 in Hunter et al) (*claim 23*) and also comprises polycrystalline silicon 42 (cf. col. 3, lines 55-62 in Hunter et al) (*claim 24*), while the first conductivity type is p-type (*claim 25*) (see above, discussion of claim 22).

On claim 26: Although neither Hunter et al nor Yamaguchi necessarily teach the further limitation as defined by claim 21, application of the device by Hunter et al and Yamaguchi et al, i.e., a MOS device with latchup protection, to power transistors is an obvious application of the invention, as is evident from Pfirsch, who teaches DMOS power transistors, while it is understood in the art that latch-up is a ubiquitous concern for MOS signal processing devices. Claim 21 thus merely recites an obvious application of the invention.

Conclusion

2. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

JPM
February 16, 2005